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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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|-------------|--|-----------------|--------------------------|
| Applicant: | DUTTA et al. | Examiner: | Unassigned |
| Serial No.: | 10/005,551 | Group Art Unit: | Unknown |
| Filed: | November 8, 2001 | Docket No.: | US018181 (VLSI.331PA) |
| Title: | HIGH-SPEED COMPUTATION IN ARITHMETIC LOGIC CIRCUIT | | |

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on _____, 2001.

By: _____

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

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Sir:

Prior to commencing substantive examination of the above-identified application on the merits, please enter the following Preliminary Amendment.

In The Specification

At page 6-7, lines 26-29 and 1-10, please replace the paragraph as follows (changes are shown on the pages attached hereto):

Another important aspect and application of the present invention is illustrated in FIG. 1 by way of a digital filtering circuit 100. The datapath unit 102 is a pipelined cascade of combinational logic circuits 110a, 110b, and including arithmetic operations such as additions, subtractions, multiplications, and/or logical operations such as AND, OR, NOT, MULTIPLEX, SHIFT. After each combinational logic circuit, a pipelined register 112a, 112b, etc. is used to feed the result of the previously-executing combinational logic circuit to the next combinational logic circuit. The datapath 102 is controlled by the control/mode processor 120 with data being fed through memory 130 for processing by the pipelined datapath unit 102 and sent out. The speed of operations depends, among many things including, for example, the clock cycle time,